General Purpose 256KBit Non-volatile Memory for Operation to 250°C

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Abstract

High-temperature non-volatile memory is needed for applications such as program memory storage for micro-controllers, high-temperature data-logging, storage of calibration coefficients for sensor compensation, etc. SOI CMOS has been proposed and demonstrated as a technology suitable for implementation of high-temperature EEPROM. However, there are presently no readily available non-volatile memory components suitable for general-purpose use above 200°C. This paper describes a high-temperature general-purpose EEPROM that has been developed for use at temperatures up to 250°C. The EEPROM is implemented in high temperature 0.8 micron SOI CMOS process, with no additional steps required for non-volatile memory capability. It employs a single-poly floating-gate memory cell that can be programmed and erased over the full operating temperature range. High-voltages for program/erase waveforms are routed to the memory elements using extended-drain transistors with elevated drain/source breakdown voltage. Previous papers have described demonstration memory in this process flow that required externally-generated program/erase waveforms. This paper describes a full-featured memory design where program/erase waveforms are generated on-chip. External capacitors are used in conjunction with charge-pumps to provide high-voltage supplies for the program/erase waveforms. The HTEEPROM is 256Kbits and may be electrically configured by an input pin as either a serial or parallel memory. The design incorporates an on-chip timer to support periodic memory refresh to extend data retention indefinitely. This design is the largest high-temperature non-volatile memory to date developed specifically for high-temperature applications.

Key words: High-temperature electronics, EEPROM, Non-volatile Memory

1.0 Introduction

In extended temperature range electronic systems there is a need for non-volatile memory. In particular re-writable EEPROM memory is needed in order to store program code for microprocessors; to configure SRAM-based Field-programmable gate arrays; to store calibration coefficients, hardware ID codes, and other application-specific parameters; and to log data. Conventional non-volatile memories generally are not specified for operation above 150°C. Limitations of conventional bulk-CMOS design platforms make it difficult to extend the operating temperature of these devices beyond about 170°C. Using design methodology optimized for high-temperature, bulk-CMOS EEPROM technology has been demonstrated for 180°C application, and tested at up to 200°C [1]. Stand-alone and embedded EEPROM devices using Silicon-on-Insulator (SOI) processes have been reported [2, 3] with operation up to 250°C. However, none of these have become commercially available.

The objective of this effort is to develop a 256Kbit general-purpose High-Temperature EEPROM (HTEEPROM) capable for operation at 250°C, and that is suitable for fabrication in a commercial SOI CMOS process. General-purpose in this case means a memory device that may be configured for either serial or parallel read/write access. In addition the HTEEPROM is intended to support configuration of an SRAM-based high-temperature FPGA that was developed concurrently. In pursuing this goal, the intent is not to develop or rely on new wafer-process technology, but rather to develop the memory within the constraints of an existing wafer-process.

This strategy expedites commercial product introduction despite low initial production volumes.

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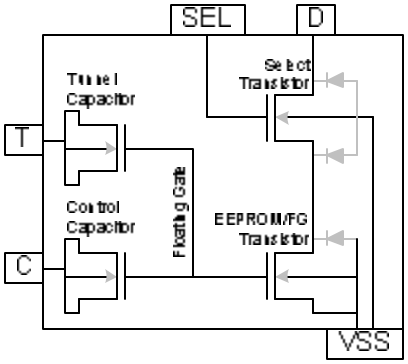
2.0 SOI Technology and Bit Cell Structure

As already noted, the HTEEPROM design is constrained by the IC fabrication process. The process flow in this case is a 5V partially depleted SOI CMOS process (see Table 1) that was developed specifically for high-temperature applications [4]. The relatively high threshold voltage is a result of implant adjustment so that the degradation in sub-threshold leakage current at high temperature does not affect the transistor "off current". The transistor off current (Vgs=0) at high temperature is purely a result of junction leakage rather than sub-threshold conduction.

Table 1: HTSOI Process Features

Process Feature	Typical Characteristic
Gate Oxide thickness	150 angstroms
Transistor length	0.8 microns (min.)
Target Vtn/Vtp 25°C 250°C	 1.2V / -1.3V 0.85V / - 1.0V
Sub-Vtslope, mV/dec 25°C 250°C	NMOS PMOS 150 180 260 320
Transistor "Off current" Nch, 250°C Pch, 250°C	 0.8 nA/micron width 0.5 nA/micron width

As in the previously cited SOI EEPROM implementations, there is only a single polysilicon layer in this process. Therefore, the memory element for the HTEEPROM is a single-poly floating-gate bit cell (Figure 1). The control capacitor is sized much larger than either the tunnelling capacitor or the floating-gate EEPROM transistor. Therefore, when voltage is applied across terminals T and C, it appears mostly across the tunnelling capacitor. By controlling this voltage, charge may be added or removed from the floating gate by Fowler-Nordheim tunnelling across the tunnel capacitor oxide.



elevated at 250°C. Dealing with this elevated leakage at extreme temperature is one of the challenges for meeting 250°C data-retention requirements (the ability to store logic state for extended periods). The elevated leakage current at 250°C reduces the length of time that charge can be reliably stored on the floating gate of the bit cell. In general it will be necessary to refresh (i.e., re-write) the data to the bit cell at intervals in the range 500 to 1000 hours if the memory is continuously operating at 250°C. Even at 250°C data retention can be significantly enhanced if the bias across the tunnelling oxide is 0V. Indeed, the bit cell of this memory was characterized on test structures for data retention [5]. In this test, the device was un-powered between test readings and it was observed that for an un-disturbed bit cell sufficient charge was stored on the floating gate to enable reliable reading after 10,000 hours at 250°C.

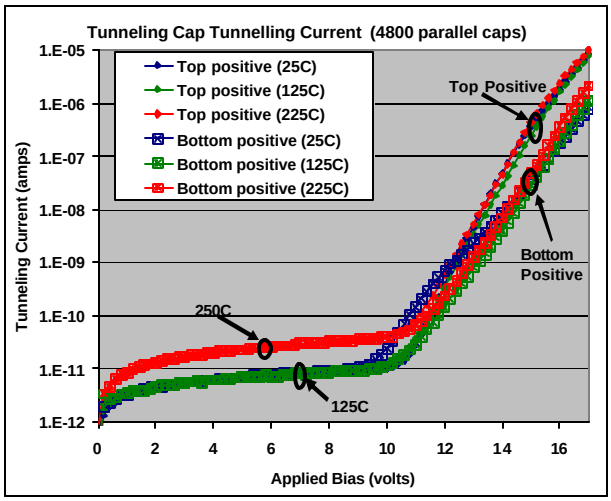
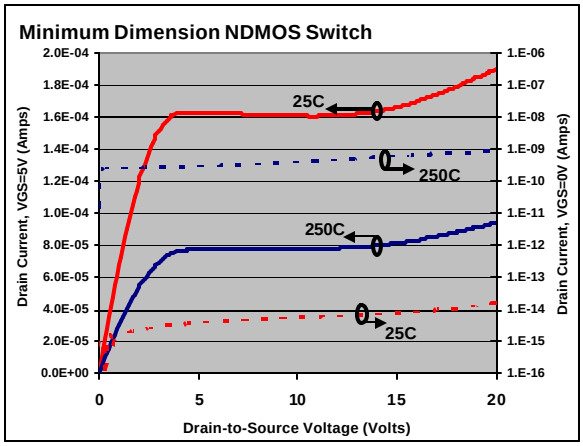


Figure 2: Tunnelling Current vs. Temperature and Voltage

Tunnelling current begins at between 9V and 11V. At higher voltages (above 14V) there is not a large difference in tunnelling current characteristics with temperature. However, there is a significant difference in the magnitude of current based on polarity of the applied bias. For this reason, the time that a voltage must be applied to transfer electrons onto the floating gate (reducing the apparent Vt) is significantly less than the time required to remove that same amount of charge. This leads to design considerations for the duration of high-voltage waveforms generated to write the memory.

Another challenge for HTEEPROM implementation is the requirement for the generation and routing of high-voltages, in excess of the 5V operating range normally employed for this technology. To generate and route these voltages extended-drain MOSFET devices (referred to at lateral DMOS) are used. The drain terminal is pulled away from the gate of the device and extended to the gate via the well-implant normally used for the opposite device type. For example, an N-channel DMOS device is fabricated with a P-well under the gate and the N-well implant (normally used for P-channel devices) is used between the gate edge and the drain terminal. This approach does not require any additional process steps.

Minimum dimension DMOS devices are used in level-shifters and as switches in the memory row and column interfaces. "ON" and "OFF" characteristics for minimum geometry layouts are shown in Figure 3. These curves show that the drain voltage can extend to 20V and that even at 250°C the ratio of on/off current spans four orders of magnitude.



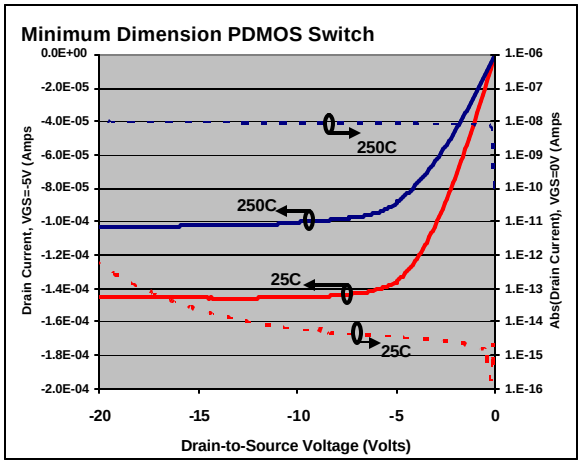


Figure 3: N-channel and P-channel extended-drain lateral DMOS "ON" Current and "Off" Leakage (Leakage normalized to minimum width)

3.0 High-temperature EEPROM Functional Approach and Demonstration

Write waveforms used to write data to the bit cell are shown in Figure 4. The SOI technology has been used to advantage in that it is practical to generate both positive and negative voltages (via charge pumps) on the chip without having to consider substrate biasing (since all of the active devices are oxide isolated). On-chip charge pumps have been designed so that when writing is performed a positive voltage (VP) and a negative voltage (VM) are generated, each with amplitude of approximately 8.5V. Voltage amplitude is set in proportion to an on-chip band-gap voltage reference that uses PMOS structures configured as lateral PNP bipolar transistors. Off-chip capacitors are used to support the multi-stage charge pump operation.

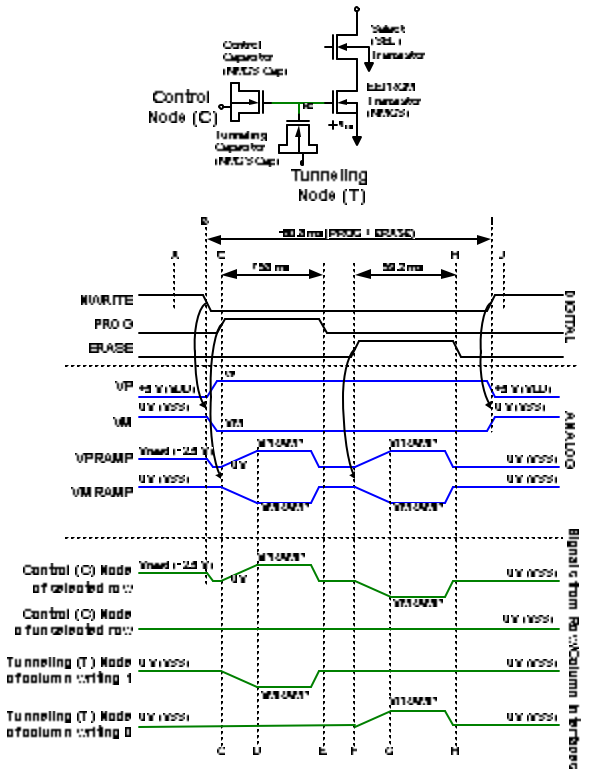


Figure 4: HTEEPROM Write Waveforms

During writing, waveforms VPRAMP and VRAMP are developed and routed to the memory array according to the scheme of Figure 4. The Control node of unselected rows remains at 0V through the writing process. The Control node of selected rows is connected first to the positive ramp voltage (VPRAMP) and then later to the negative ramp voltage (VMRAMP). In selected columns The Tunnelling node is also alternately connected to VMRAMP and VPRAMP as shown in Figure 4.

This approach enables the generation and routing of voltage through most of the array that, at 8.5V or less, are below the tunnelling voltage and therefore do not significantly disturb cells that are not being written. For cells that <u>are</u> being written, voltages are applied across the tunnelling capacitor that are approximately 14.5V (after accounting for voltage reduction according to the capacitance ratios of the Control vs. the Tunnelling capacitor and floating gate transistor). This voltage is sufficient for tunnelling. Note that the dwell times of the write waveforms are controlled so that writing a "0" (positively shifting the Vt of the floating gate transistor) is given 7x the dwell time as writing a "1" (negatively shifting the Vt of the floating gate transistor). The total duration of each write operation is approximately 60 milliseconds.

The amplitude and dwell time of these waveforms were established and characterized using a 32Kbit (4K x 8) demonstration memory (Figure 5). This device contained a complete 512 x 64 array of memory cells with row/column decoding and high-voltage interfaces. Write waveforms and control signals were generated off-chip for this demonstration. This chip allowed for data retention testing, as well as memory cycling (durability testing) and testing of the read-out circuitry (sense amps and references).

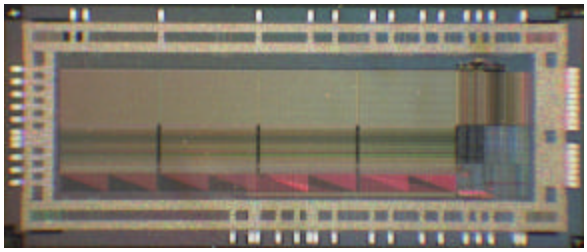


FIGURE 5: 32Kbit (4K by 8) Demonstration Memory

It is well known that floating gate memory devices that employ Fowler-Nordheim or hot-electron tunnelling exhibit degraded write capability with the accumulation of program/erase cycling. This is observed as a diminished capability for charge transfer through the tunnelling oxide. This limits the number of cycles that can be applied to a given bit-cell consistent with reliable data storage.

In developing a high-temperature EEPROM, it is necessary to consider the additive combined effect on read-out from both data cycling

(durability) as well as charge leakage (data retention) at 250°C. Data retention can also be impacted by the bias conditions during the idle state. As noted in the discussion of tunnelling current (see Figure 2) a powered idle condition with voltage applied across the tunnelling capacitor results in leakage that is elevated relative to an zero-bias or un-powered state. The question of bias during an idle state is relevant to the access time of the memory. For lowest read-access time it would be preferred that the read voltage (approximately 2.2V) be applied to the Control nodes of all of the rows of the memory array while it is in an idle state (rather than waiting to charge and settle the read voltage on an address change). In other words, there is a trade-off between read-access time and powered data retention at high-temperature.

Figure 6 summarizes the combined effect of 250°C data retention and the number of program/erase cycles. Memory cells were written a total of 100,000 times (alternating 1 and 0) using a total voltage for writing of 16.5V (plus/minus 8.25V applied across the Control and Tunnelling nodes). Dwell times were set to give a symmetric Vt shift that was initially plus/minus 1.35V (for writing 0/1 respectively). It can be seen that after 3 weeks at 250°C there is still significant Vt shift (>1.2V, or plus/minus 600mV) that can be reliably sensed through the read-out circuitry. Separate testing under power with/without read-bias voltage applied to the Control node resulted in an additional 150mV to 200mV of Vt-shift lost when the read-bias voltage is continuously applied to the control node. Other rows of these same devices were cycled 1 million times and successfully read after 537 hours at 250°C (un-powered data retention testing).

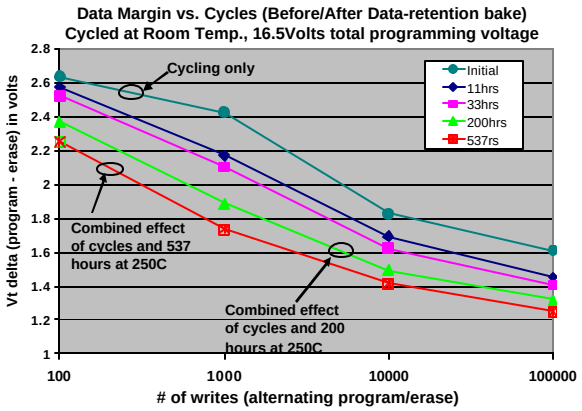


FIGURE 6: Data Retention and Data Cycling Results from 32Kbit Demonstration Memory

The demonstration memory also includes test modes where the entire memory can be addressed simultaneously for cycling tests of the bit cells. Entire arrays of the 32Kbit memory were cycled (alternately writing 1's and 0's) for 100,000 cycles without any bit-errors detected. Note that these cycling tests were performed at room temperature.

Time-dependent dielectric breakdown (TDDB) is an additional consideration for the HTEEPROM development. The HTEEPROM employs a CMOS SOI process with 150 angstrom gate oxide that is used primarily for 5V applications. During the write process large areas of gate oxide within the HTEEPROM are stressed with voltages in excess of 5V. This is in addition to the bit cells being written (for example, all of the tunnelling capacitors in cells that are not being written). For the final 256Kbit HTEEPROM design, each write operation involves stressing approximately 418,000 square microns of gate oxide at 8.5V for up to 60msec.

Large area gate-oxide test structures were tested for time-dependent breakdown as a function of applied voltage at 125°C and 250°C. Results are summarized in Figure 7. Extrapolating from the accelerated test conditions to 8.5V predicts over 2000 hours at 8.5V. This time is equivalent to the cumulative stress of 120 million write operations. Note that the area of the oxide stressed in these tests represents approximately 40% of the total area that would be stressed during a write operation of the 256Kbit EEPROM. These results are preliminary, and were intended to establish the bias conditions for subsequent 250°C testing with a larger sample size, and at bias conditions closer to actual use conditions. This additional testing is in progress at the time of this writing.

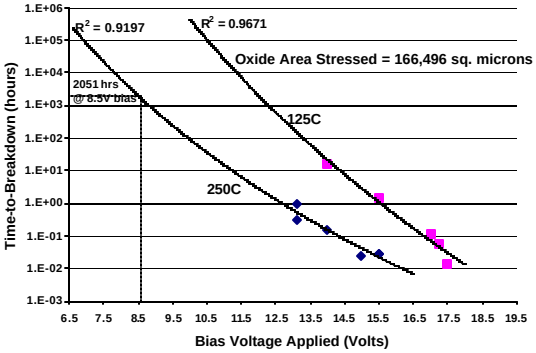


Figure 7: Gate-oxide time dependent breakdown for 166,496 square micron gate oxide test structures

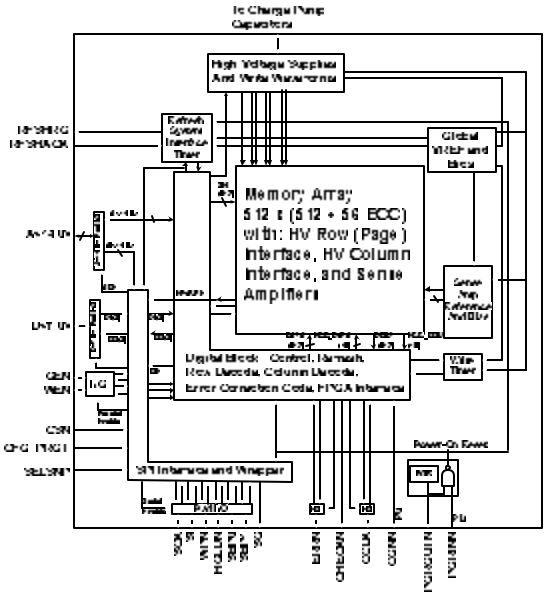
4.0 HTEEPROM Product Configuration

A complete 32K x 8 HTEEPROM product configuration has been designed and fabricated in accordance with the technology concepts, bit cell structure and operating principles already discussed. An overview of the product architecture and I/O signals is shown in Figure 8. The memory array includes 512 columns of data storage elements plus an additional 56 columns used for Error-Correction Coding (ECC). The ECC corrects for single-bit errors within a page, where a page consists of 64 bytes within a given row (1 byte = 8 bits). A digital logic block provides parallel mode access where the memory may be addressed and asynchronously read as a 32K by 8-bit memory. Worst-case parallel mode access times at high-temperature are expected to be 150nsec. The parallel interface incorporates the functionality of industry standard 28C256 parallel memories, including page buffer and control sequencing for both page-mode and byte-mode writing schemes.

All of the reference and bias voltages, timers, and write-control circuitry is included on-chip, with the exception of charge-pump capacitors. These are off-chip in order to preserve die area and ensure sufficient charge storage to operate in the presence of leakage current at 250°C.

A memory-refresh strategy is employed to enable long-term data storage at 250°C. A memory refresh-request pin goes high on power-up and approximately every 30 days thereafter to request memory refresh. If this signal is acknowledged via a refresh-acknowledge input then the memory will re-write itself in 512 sequential page-write operations. The refresh requires approximately 31 seconds to be completed. Note that this refresh is optional and may be ignored by the system. The initial power-on refresh requests "expires" after approximately 20 seconds if it is not acknowledged. In addition, due to the page-mode writing scheme, writing to any byte within a page effectively refreshes the entire page.

The parallel mode configuration includes six I/O that are dedicated for use with the High-Temperature FPGA. These I/O serve as control signals enabling the HTEEPROM to be used to load and verify configuration for a high-temperature FPGA that was developed concurrently with the HTEEPROM. Configuration of the FPGA can require up to half of the HTEEPROM capacity. Once the configuration is complete the device reverts to the standard parallel-mode operation and the remaining HTEEPROM capacity may be used by the system for other purposes. A configuration-protect pin provides for hardware write-protection of the lower half of the HTEEPROM address space, which would be that portion normally used for FPGA configuration.



- **Serial / Parallel control, and Configuration Protect input**
- **28C256 Functionally Equivalent Parallel Interface**
- **25C256 Functionally Equivalent Serial Interface**
- **High Temperature FPGA Configuration Interface**
- **Periodic refresh request timer and hand-shake control**
- **External ceramic chip capacitors support charge pumps for write operations**

FIGURE 8: HTEEPROM Architecture and Top-level Interfaces

Serial-mode operation can be invoked by a Serial/Not-Parallel configuration pin. If this pin is pulled high, then the memory is accessible for read/write access as a serial device via SPI interface in accordance with industry standard 25C256 serial memories.

The complete 256Kbit HTEEPROM product design has recently completed fabrication. A die photo is shown in Figure 9. Verification testing is on-going. As sufficient testing is successfully completed the intention is to develop commercial product specifications that support 250°C operation, production test development, and package development. It is expected that this design will be commercialized in the form of

deliverable die as well as in hermetically sealed ceramic packages suitable for 250°C.

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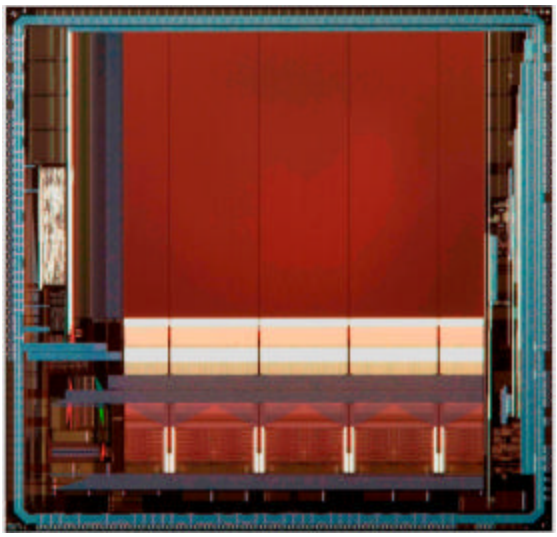

FIGURE 9: HTEEPROM Die Photo
Die Size is 12.3mm x 12.7mm

5.0 Summary and Conclusions

A commercial high-temperature SOI CMOS process flow has been shown to be capable for the development of a High-temperature floating-gate non-volatile memory element, without requiring the addition of process steps or special features. This has been shown through the characterization of tunnelling current and high-voltage device capability, and by the development and data retention testing of bit-cells.

Operating principles for a complete HTEEPROM product based on the floating gate memory elements have been developed and verified by the fabrication and testing of a 32Kbit demonstration memory. This includes date additional data retention and data-cycling tests at room temperature and at 250°C. Results indicate that the approach can support millions of write operations and at least 100,000 program/erase cycles for each of the individual bits within the memory.

Finally, a complete product configuration has been designed and fabricated as a 256Kbit HTEEEPROM. A data refresh scheme and Error-correction Coding are employed to ensure reliable long-term data storage and read-out at up to 250°C. The design is flexible to support both serial and parallel mode read and write operation, and incorporates an FPGA loader to automatically download configuration data into an SRAM-based FPGA. Design verification of this product configuration is a current task, to be followed by development of high-temperature packaging, screening tests, and datasheets suitable for commercial product offering.

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